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	Filing Date	Dec 20, 2001	
	First Named Inventor	Tomsio, Nayon	
	Group Art Unit	Unassigned	
	Examiner Name	Unassigned	
Total Number of Pages in This Submission		Attorney Docket Number	P6459/SUN-01-02

ENCLOSURES (check all that apply)		
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2/11/02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Tomsio et al.

Serial No: 10/028,814

Filed: December 20, 2001



PATENT APPLICATION

Group Art Unit: Unassigned

Examiner: Unassigned

For: RESISTIVE VIAS FOR CONTROLLING IMPEDANCE AND
TERMINATING I/O SIGNALS AT THE PACKAGE LEVEL

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Information Disclosure Statement

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Sir:

The following information is submitted in compliance with Applicants' duty of disclosure under 37 C.F.R. § 1.56. A copy of each of the twelve (12) references recited below accompanies this document.

PATENT DOCUMENTS

<u>Patent Number</u>	<u>Inventor</u>	<u>Grant Date</u>
3,210,831	Johnson et al.	Oct. 12, 1965
4,179,797	Johnson	Dec. 25, 1979
4,300,115	Ansell et al.	Nov. 10, 1981
5,164,699	Smith et al.	Nov. 17, 1992
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5,808,478	Andresen	Sep. 15, 1998
5,898,321	Ilkbahar et al.	Apr. 27, 1999
6,100,787	Huang et al.	Aug. 8, 2000
6,115,298	Kwon et al.	Sep. 5, 2000

PATENT DOCUMENTS CONTINUED

<u>Patent Number</u>	<u>Inventor</u>	<u>Grant Date</u>
6,130,601	Brown et al.	Oct. 10, 2000
6,246,312	Poole et al.	Jun. 12, 2001

NON-PATENT DOCUMENTS

The Effects of Vias on PCB Traces, Design Note, UltraCAD Design, Inc., 1994.

CERTIFICATE OF MAILING

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Respectfully submitted,



Kenneth C. Brooks
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